Electronic Version
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Claims

[c1] What is claimed is:

1. A substrate isolation design, comprising:

a P substrate;

a P well positioned on the substrate;

at least a device positioned in the P well; and

at least a P substrate guard ring surrounding the device.

[c2] 2. The substrate isolation design of claim 1, wherein the P substrate guard ring is positioned beneath a shallow isolation trench formed within the P well.

[c3] 3. The substrate isolation design of claim 1, further comprising at least a P+ guard ring surrounding the device.

[c4] 4. The substrate isolation design of claim 3, wherein the P+ guard ring is between the device and the P substrate guard ring.

[c5] 5. The substrate isolation design of claim 4, further comprising at least an N well guard ring between the P+ guard ring and the P substrate guard ring.

[c6] 6. The substrate isolation design of claim 5, further

comprising at least a deep N well guard ring positioned beneath the P well to contact to the N well guard ring.

[c7] 7. The substrate isolation design of claim 1, further comprising an N well guard ring surrounding the device.

[c8] 8. The substrate isolation design of claim 7, wherein the N well guard ring is between the device and the P substrate guard ring.

[c9] 9. The substrate isolation design of claim 8, further comprising at least a deep N well guard ring positioned beneath the P well to contact to the N well guard ring.

[c10] 10. A substrate isolation design, comprising:
a substrate;
at least a device positioned on the substrate;
a first guard ring surrounding the device;
a second guard ring surrounding the first guard ring; and
a third guard ring surrounding the second guard ring, the third guard ring being a substrate guard ring.

[c11] 11. The substrate isolation design of claim 10, wherein the first guard ring comprises a P+ guard ring.

[c12] 12. The substrate isolation design of claim 10, wherein the second guard ring comprises an N well guard ring.

[c13] 13. The substrate isolation design of claim 10, wherein the third guard ring comprises a P substrate guard ring.

[c14] 14. The substrate isolation design of claim 10, wherein the substrate guard ring is positioned beneath a shallow isolation trench.

[c15] 15. The substrate isolation design of claim 10, further comprising at least a deep N well guard ring connecting to the N well guard ring.

[c16] 16. A substrate isolation design, comprising:
a P substrate;
at least a device positioned in the substrate; and
at least a P substrate guard ring surrounding the device.

[c17] 17. The substrate isolation design of claim 16, further comprising at least a shallow isolation trench surrounding the device, and wherein the P substrate guard ring is positioned beneath the shallow isolation trench.

[c18] 18. The substrate isolation design of claim 16, further comprising at least a P+ guard ring positioned between the device and the P substrate guard ring.

[c19] 19. The substrate isolation design of claim 18, further comprising at least an N well guard ring between the P+ guard ring and the P substrate guard ring.

[c20] 20. The substrate isolation design of claim 19, further comprising at least a deep N well guard ring contacting to the N well guard ring.

[c21] 21. The substrate isolation design of claim 16, further comprising an N well guard ring positioned between the device and the P substrate guard ring.

[c22] 22. The substrate isolation design of claim 21, further comprising at least a deep N well guard ring contacting to the N well guard ring.